

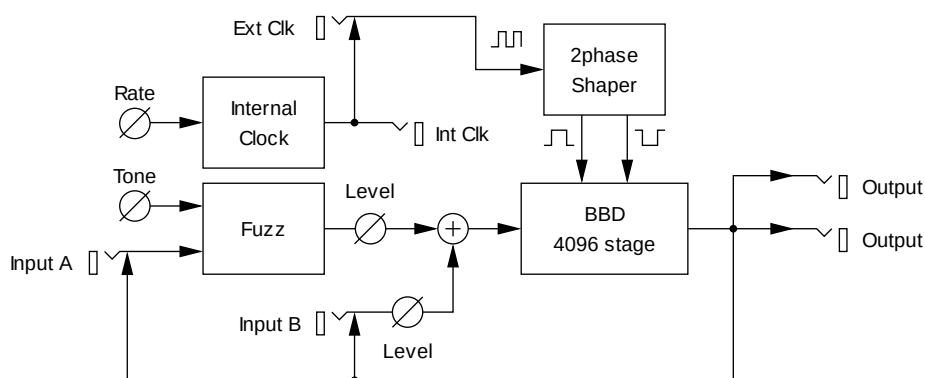
Fuzz Bucket

Version: 1.1

Date: 2018-08-11

The Fuzz Bucket is an 8HP eurorack fuzz and delay module made up of a two transistor fuzz circuit and an MN3005 bucket brigade delay (BBD). Unlike most delay implementations which aim to mask sampling and reconstruction error, the Fuzz Bucket provides direct unfiltered access to delay line inputs and outputs as well as override of the BBD clock. All of the aliasing, distortion, and clock noise peculiar to bucket brigade delay is celebrated as a primary effect instead of being hidden away as an unwanted problem. In addition, a silicon "fuzz face" is grafted onto one of the audio inputs, to add some extra colour.

Overview



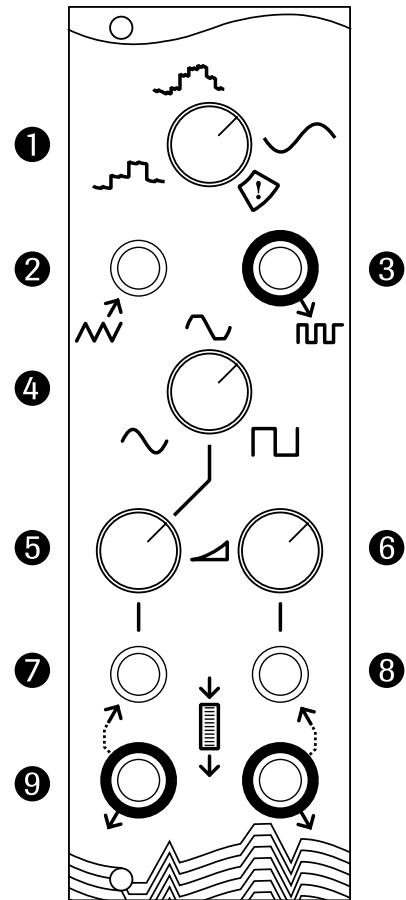
Two audio inputs are scaled and mixed before being fed into a 4096 stage delay line. Input channel A passes through a two transistor fuzz circuit, while input channel B is passed through unmodified. When nothing is patched into an input, it is fed with a copy of the module output.

A two-phase clock drives the bucket brigade delay line from an input signal at one half the frequency input. When no external clock signal is patched in, an internally generated clock signal is used.

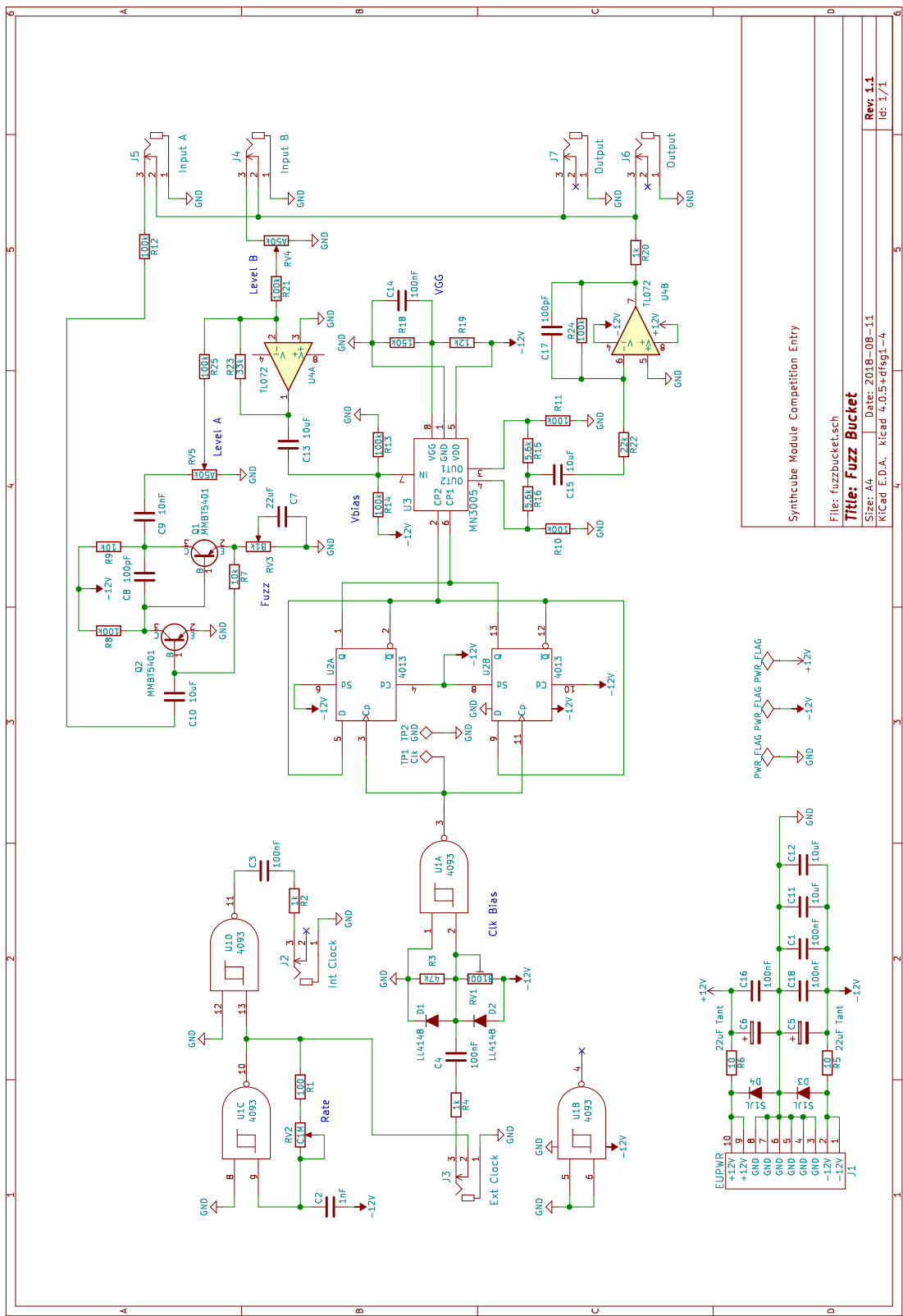
For a brief demo of some simple connection examples, see the [Fuzz Bucket Demo Video](#).

Controls & Connections

1. Internal rate control - sets the rate of the internal clock generator from roughly 3kHz to 3MHz. Above 200kHz (roughly 4 o'clock position), the MN3005 BBD is overclocked.
2. External clock override - AC coupled BBD clock override input. Any signal with at least 2V of swing between high and low values can be used. Note that the BBD frequency is one half that of the input clock. When no connector is present, the internal clock is routed to the BBD.
3. Clock output - outputs a copy of the internal clock, even when an external override is present.
4. Input A fuzz amount - controls how much fuzz is applied to the signal on input A.
5. Input A level - adjusts the level of fuzzed signal from input A that is fed into the delay line.
6. Input B level - adjusts the level of clean signal from input B that is fed into the delay line.
7. Input A - AC coupled signal input routed through a fuzz circuit before being fed into the delay line. When no connector is present, this input is shorted to the module output.
8. Input B - AC coupled signal input fed into the delay line. When no connector is present, this input is shorted to the module output.
9. Outputs - Two copies of the module output.



Schematic



Parts

Qty	Value	Refs	Footprint	Note	Example Part
2	10	R5 R6	R_0805	1/4W	ERJ-T06J100V
1	100	R1	R_0805		ERJ-6ENF1000V
3	1k	R2 R4 R20	R_0805		ERJ-S06F1001V
2	5.6k	R15 R16	R_0805	1%	ERJ-6ENF5601V
2	10k	R7 R9	R_0805		ERJ-S06F1001V
1	12k	R19	R_0805	1%	ERJ-6ENF1202V
1	22k	R22	R_0805		ERJ-6ENF2202V
1	33k	R23	R_0805		ERJ-6ENF3302V
1	47k	R3	R_0805		ERJ-6ENF4702V
9	100k	R8 R10 R11 R12 R13 R14 R21 R24 R25	R_0805	1%	ERJ-U06F1003V
1	150k	R18	R_0805	1%	ERJ-6ENF1503V
2	100pF	C8 C17	C_0805	COG $\geq 25V$	08053A101FAT2A
1	1nF	C2	C_0805	COG $\geq 25V$	C0805H102J3GACT1K0
1	10nF	C9	C_0805	COG $\geq 25V$	GRM2195C1H103JA01D
6	100nF	C1 C3 C4 C14 C16 C18	C_0805	$\geq 25V$	GCE21BR71H104KA01L
5	10uF	C10 C11 C12 C13 C15	C_0805	$\geq 25V$	GRM21BC71E106KE11L
1	22uF	C7	C_0805	$\geq 25V$	GRT21BR61E226ME13L
2	22uF	C5 C6	CP_2312	$\geq 20V$ Tantalum	F971D226MCCHT3
2	LL4148	D1 D2	D_SOD80		LL4148
2	S1JL	D3 D4	D_SMF		S1JL
2	MMBT5401	Q1 Q2	SOT-23		MMBT5401
1	4093	U1	SOIC-14		HEF4093B
1	4013	U2	SOIC-14		CD4013BM
1	TL072	U4	SOIC-8		TL072CDR
1	MN3005	U3	MN3005		
2		TP1 TP2	Testpoint	Optional	151-202-RC
1	B100k	RV1	3306F		3306F-1-104
1	B1k	RV3	Alpha9mmSG		RD901F-40-15R1-B1K
2	A50k	RV4 RV5	Alpha9mmSG		RD901F-40-15R1-A50K
1	C1M	RV2	Alpha9mmSG	B or C ok	RD901F-40-15R1-C1M
4	Knob				
1		J1	IDC_2x05		87834-1019
6		J2 J3 J4 J5 J6 J7	Thonkiconn		WQP-PJ398SM

Component Selection Notes

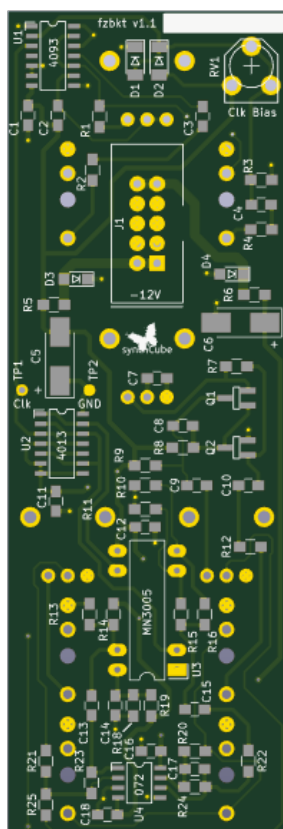
An HEF4093 quad CMOS NAND IC was chosen for schmitt trigger U1 for a low typical hysteresis voltage of about 1V. This selection allows for a wide range of clock sources without the need for amplification. Any 4093 equivalent should work, but may require a larger clock input to reliably switch.

The overall gain of the delay block is set by resistors R23 and R22. Resistor R23 reduces the level of the input so that the BBD will clip when the input signal at R21 and R25 exceeds approximately 10V peak to peak. Output resistor R22 reverses this attenuation and adds a small amount of gain to allow self-oscillation.

Capacitor C17 is required to reduce high frequency ringing on the output which is triggered by spikes that appear at the BBD output as it switches between buckets. The value of 100pF provides a compromise between suppression and reduced bandwidth.

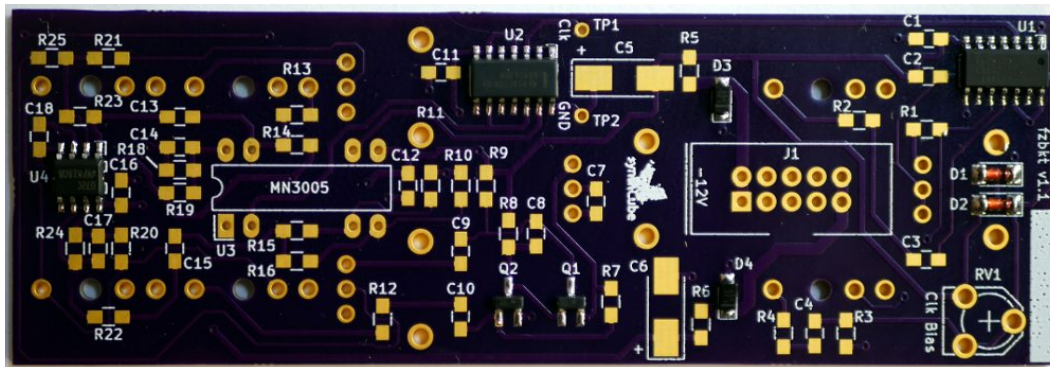
Fuzz transistors Q1 and Q2 were selected arbitrarily for availability, low gain and poor noise performance. Capacitor C8 helps to suppress unpleasant oscillation and AM radio pickup at high values of fuzz.

Circuit Board & Front Panel Layout

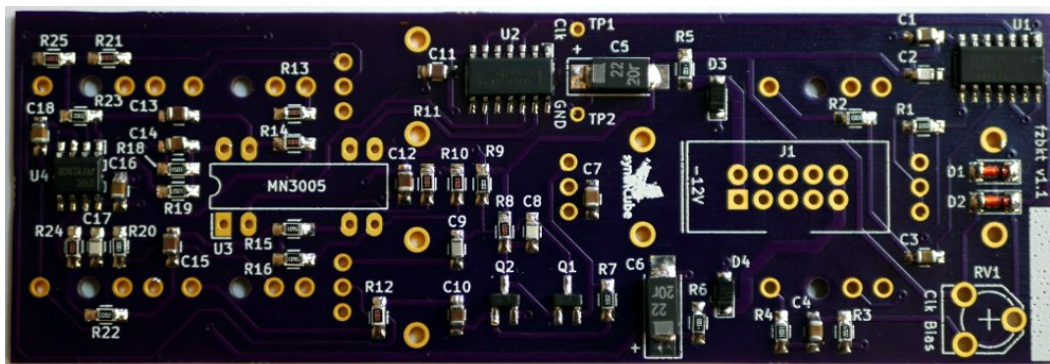


Build Instruction

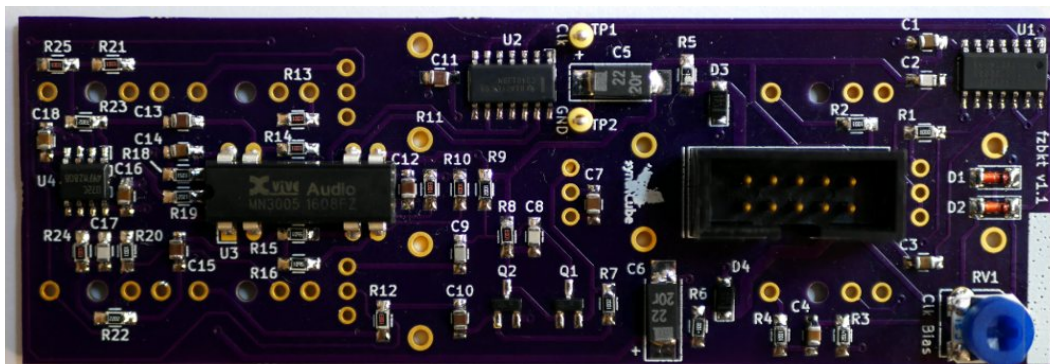
- Clean PCB and inspect for defects.
- Solder transistors Q1 & Q2.
- Solder ICs U1, U2 & U4. Pin one on each chip is indicated on the silkscreen.
- Solder diodes D1, D2, D3 & D4.



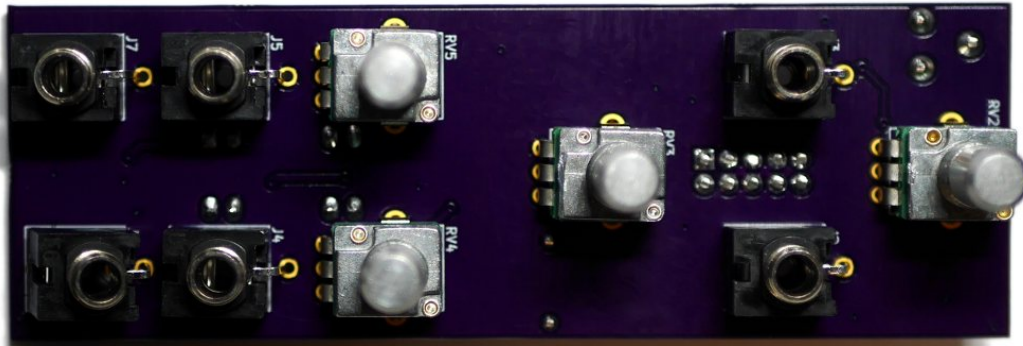
- Solder all 0805 resistors.
- Solder all 0805 capacitors.
- Solder Tantalum capacitors C5 & C6, ensure orientation matches silkscreen.



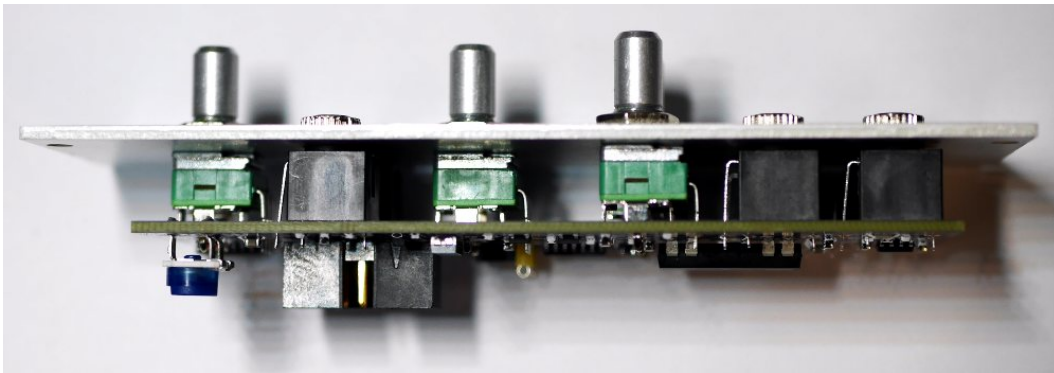
- Clean board and inspect solder joints.
- Solder MN3005 bucket brigade IC U3.
- Solder RV1 (Clk Bias) trimmer.
- Optionally, solder test points TP1 & TP2.
- Solder power header J1.
- Clean board and check solder joints.



- Insert pots RV2, RV3, RV4 & RV5 and jacks J2, J3, J4, J5, J6 & J7 according to silkscreen.



- Fit front panel and lightly attach all parts.
- Ensure flush connection with PCB and panel, then solder all jacks and pots.

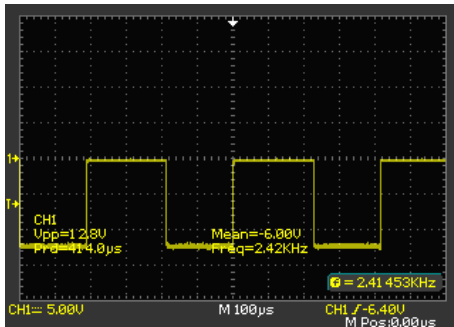


- Clean board, tighten jacks and pots, then attach knobs.

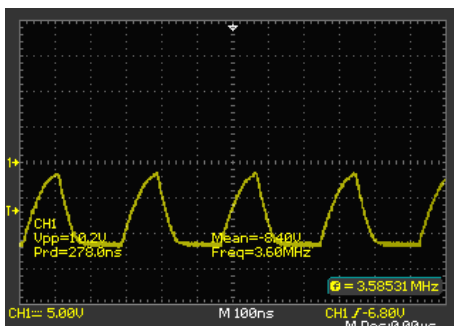


Test and Adjustment Procedure

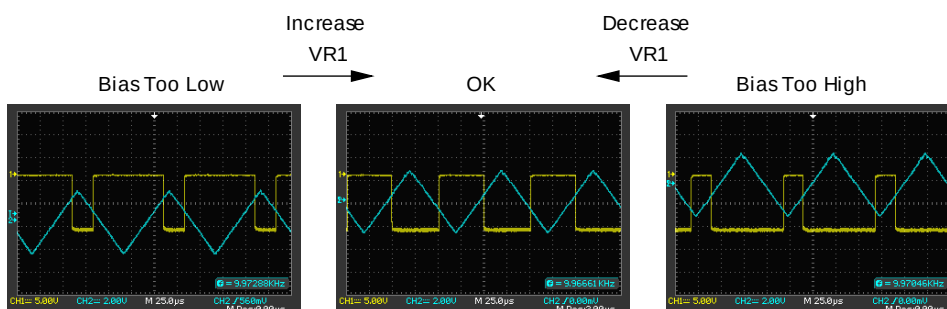
- Set all controls to minimum, fully counter-clockwise.
- Set RV1 (Clk Bias) trimmer to mid-point.
- Connect an oscilloscope to test point TP1 (Clk).
- Verify that the internal clock is generating a square wave running at approximately 3kHz.



- Vary rate control and check that the internal clock increases to roughly 3MHz at maximum (fully clockwise) position. When in maximum position, the waveform may be attenuated and appear triangular - this is normal.

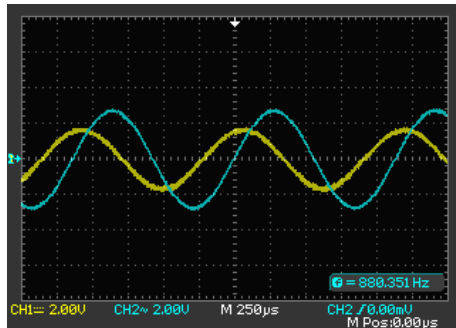


- Connect a 5V peak to peak, roughly 10kHz triangle wave to the Ext Clk input.
- Adjust RV1 (Clk Bias) until the observed waveform is close to 50% duty cycle.

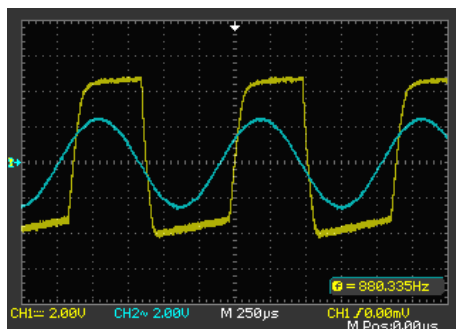


- Disconnect Ext Clk input and set rate control so the internal clock is running at roughly 200kHz (about 4 o'clock position).
- Connect a 5V peak to peak 1kHz sine wave to input A.
- Connect one module output to an oscilloscope.
- Adjust input A level to about 3 o'clock position.

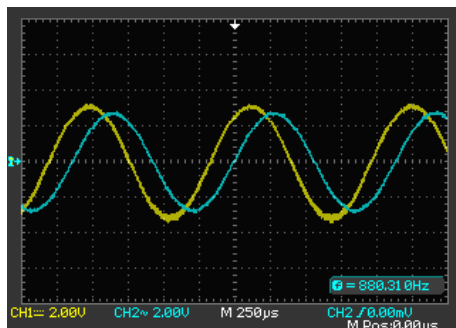
- Verify roughly 4V peak to peak sinusoidal wave on output.



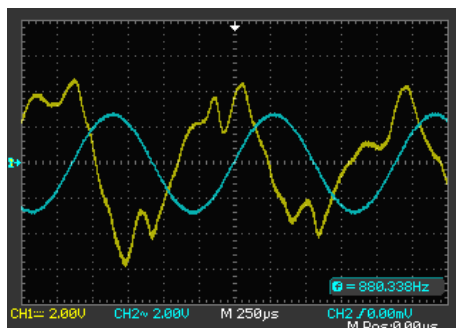
- Vary fuzz amount control and verify clipping of input signal.



- Set input A level to minimum, and swap input signal from A to B.
- Adjust input B level to maximum (fully clockwise) setting.
- Verify roughly 6V peak to peak sinusoidal wave on output.



- Test feedback by increasing input A level, then vary rate for effect.



Design Files

- Schematic Diagram: [PDF](#)
- Parts List: [CSV](#)
- PCB Gerber Files: [ZIP](#)
- Kicad project: [Gzipped TAR](#)
- Sample front panel design: [Inkscape SVG](#)
- Front panel drill guide: [PDF](#)

Issues and Limitations

Unfiltered outputs from the BBD carry a small amount of the clock signal, and at near ultrasonic rates this clock noise may be perceived as a loud hiss. Passing the output of the module through a low pass filter can help to suppress the clock, and eliminate the hiss sound. When driving the BBD from a VCO, a low pass VCF with cutoff set to track the VCO roughly three octaves below the oscillator rate will reduce most of the clock noise. Note that while this will suppress clock noise and some of the output error, aliasing will still occur if the input signal contains frequencies greater than half the BBD clock rate (one quarter of the external clock input).

Since the output and inputs are shorted together when nothing is patched, insertion of a patch lead will temporarily connect the input signal directly to the output, and connecting to the output may mute an incoming signal briefly. In order to keep the circuit design as simple as possible, these transient patching issues have not been addressed.

While the fuzz circuit was derived from a fuzz face layout, adaptation to eurorack levels and power has changed the way it clips, particularly at low input levels. Instead of asymmetrically clipping the positive and negative signal, the circuit will clip both equally. This behaviour is quite unlike that of the fuzz face, but it works adequately in this context.

Further Work

In the design presented above, the MN3005 operates between 0V and -12V, requiring AC coupled input and output. By using a pair of linear regulators and trimming the output offset, it should be possible to run the MN3005 on a balanced local power supply, and DC couple both input and output. This change would allow use as a control voltage delay, which when used with feedback could be quite interesting.

Based on tests of the prototype module with other instruments, many of the most satisfying patches involve overriding the BBD clock with a sequenced VCO. By providing a direct clock override, the work of generating an interesting clock has been avoided and the circuit kept as simple as possible. It might be worthwhile to extend the clock circuit either with a precision VCO like the CEM3340 or a PLL like the 4046. This could then be paired with an output filter designed to track and suitably suppress clock noise automatically.

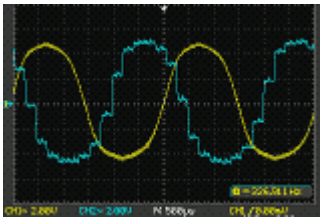
Acknowledgements

The fuzz block applied to input A is a crude adaptation of the classic two transistor fuzz face circuit as published on [ElectroSmash](#) utilising notes on the use of silicon transistors in [The Technology of the Fuzz Face](#) by R. G. Keen.

The delay core and the two-phase clock that drives it is based on a circuit published in Barry Klein's Electronic Music Circuits.

PCB footprints and schematic symbols are derived from the Kicad official repositories, or created from scratch - these have been included in full within the [Kicad project](#).

Many thanks to Adam Cole for his help with design and testing, and for listening patiently to dumb ideas. Thanks also to Morgan McWaters, Lewis Boyes and the team at Found Sound for their support and encouragement.



Nathan Fraser, August 2018